FIG. 1

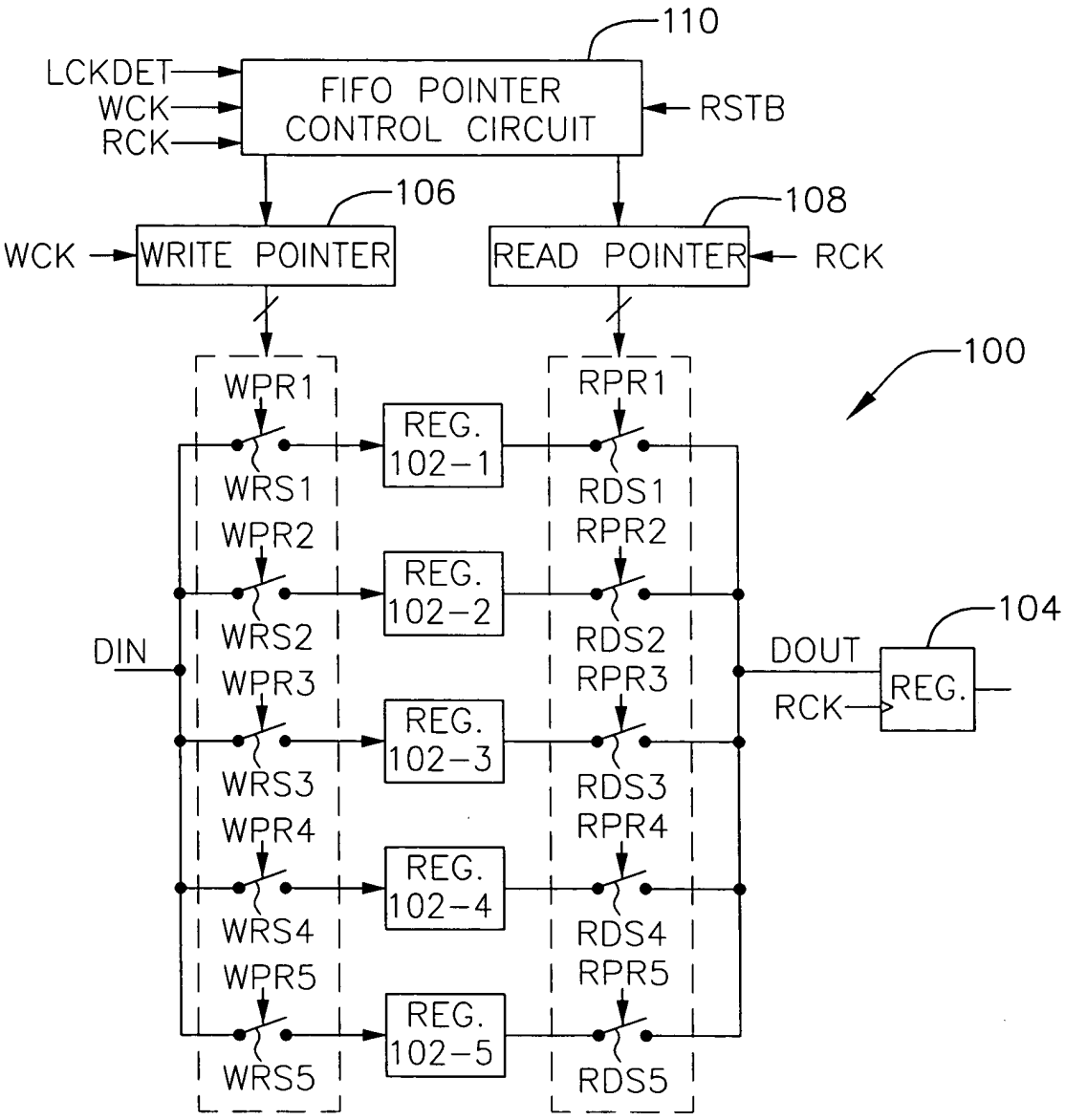

110
LCKDET
WCK
RCK
FIFO POINTER CONTROL CIRCUIT
RSTB
106
108
WCK
WRITE POINTER
READ POINTER
RCK
100
WPR1
RPR1
REG. 102-1
WRS1
RDS1
WPR2
RPR2
REG. 102-2
104
DIN
WRS2
RDS2
DOUT
WPR3
RPR3
REG.
RCK
REG. 102-3
WRS3
RDS3
WPR4
RPR4
REG. 102-4
WRS4
RDS4
WPR5
RPR5
REG. 102-5
WRS5
RDS5

FIG. 2

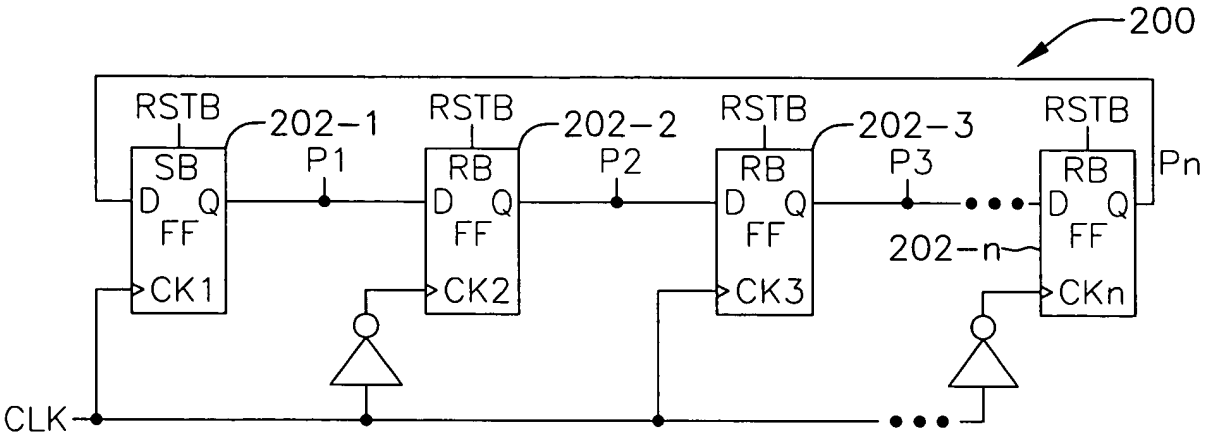


FIG. 3

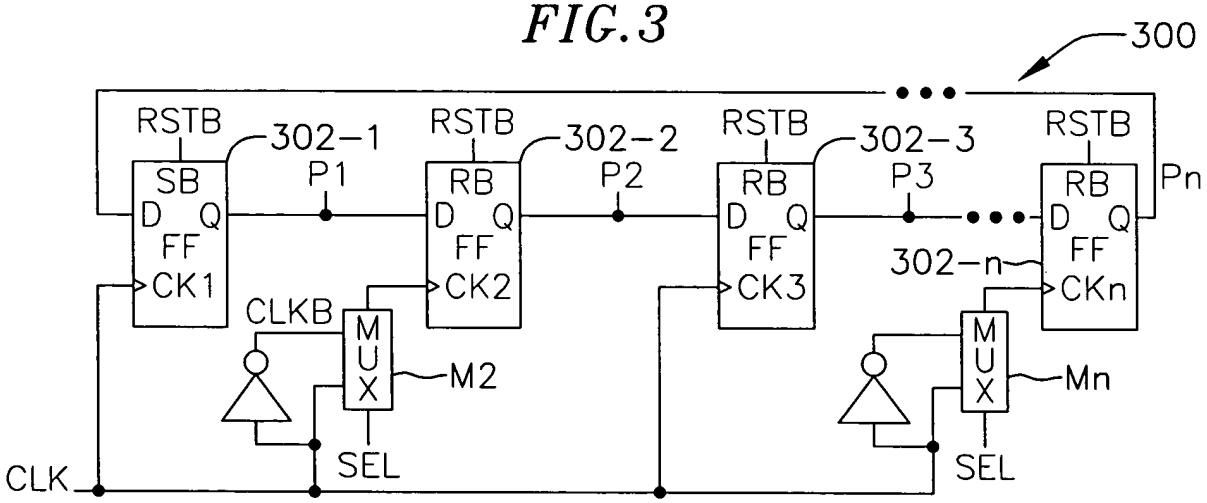


FIG. 4

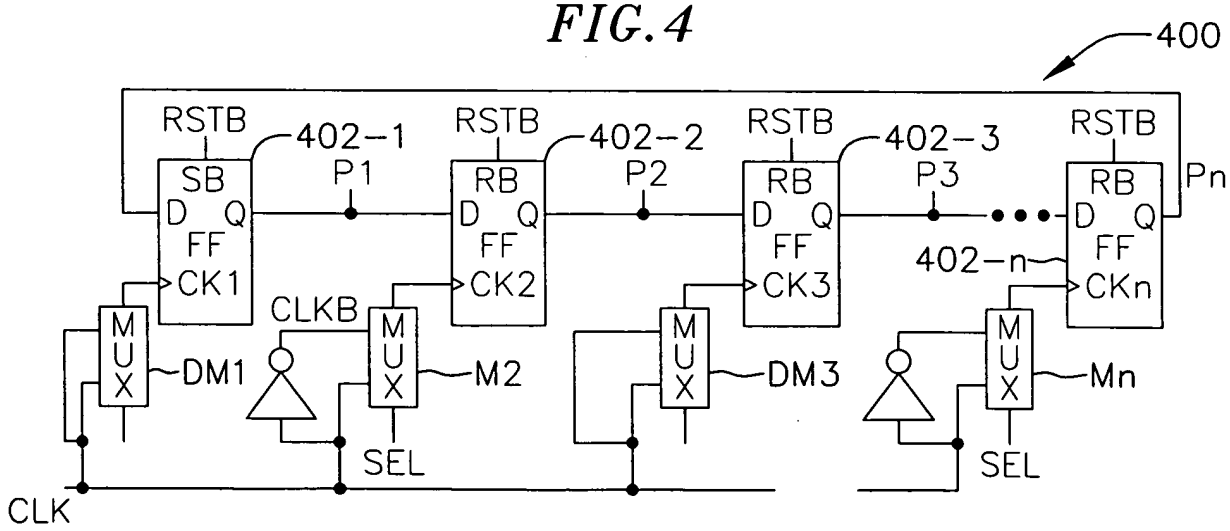
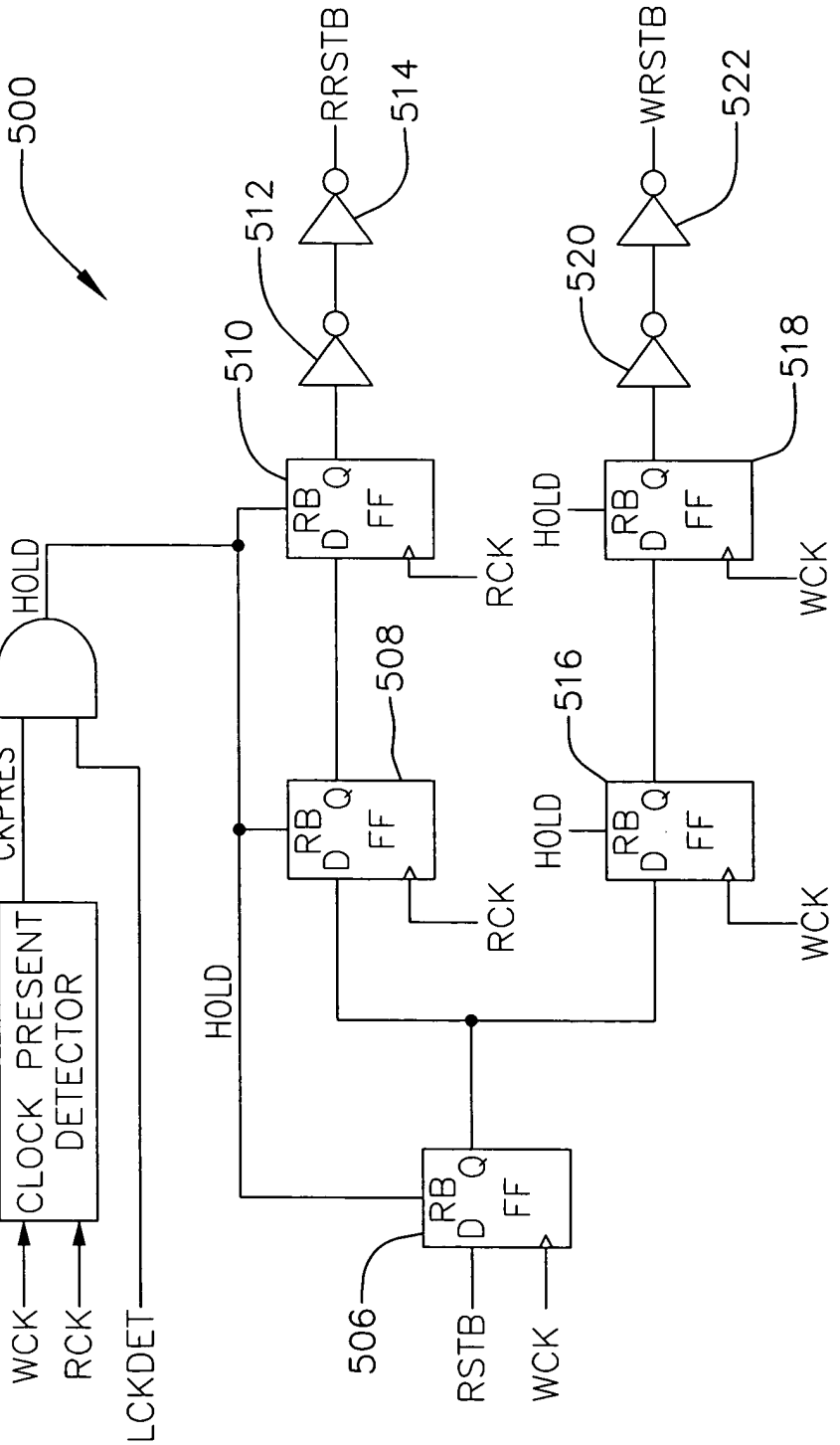


FIG. 5


500
502
CLOCK PRESENT DETECTOR
504
HOLD
CKPRES
WCK
RCK
LCKDET
506
RSTB
WCK
HOLD
508
510
512
RRSTB
514
RB
D
Q
FF
RCK
516
518
520
522
WRSTB
WCK

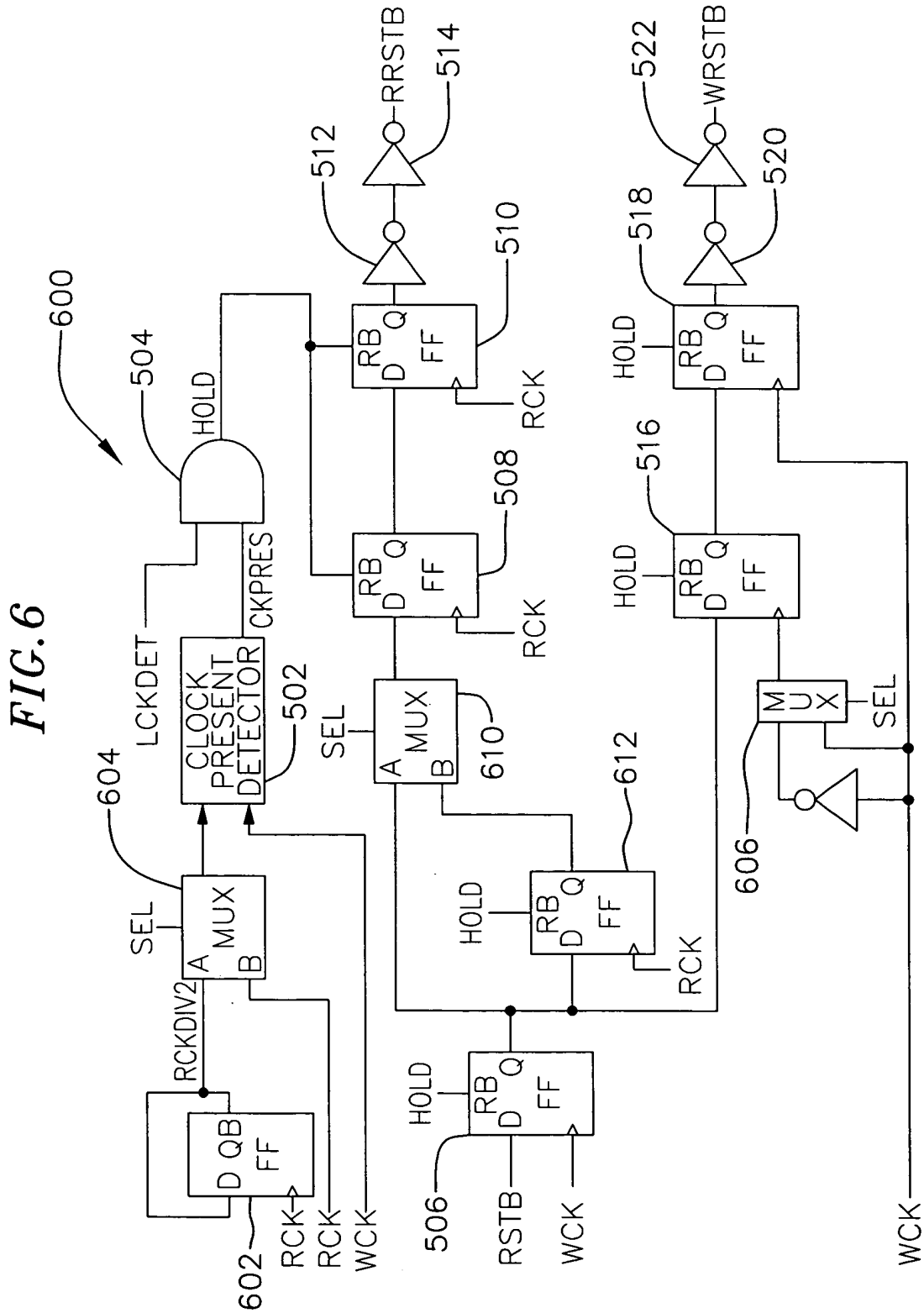
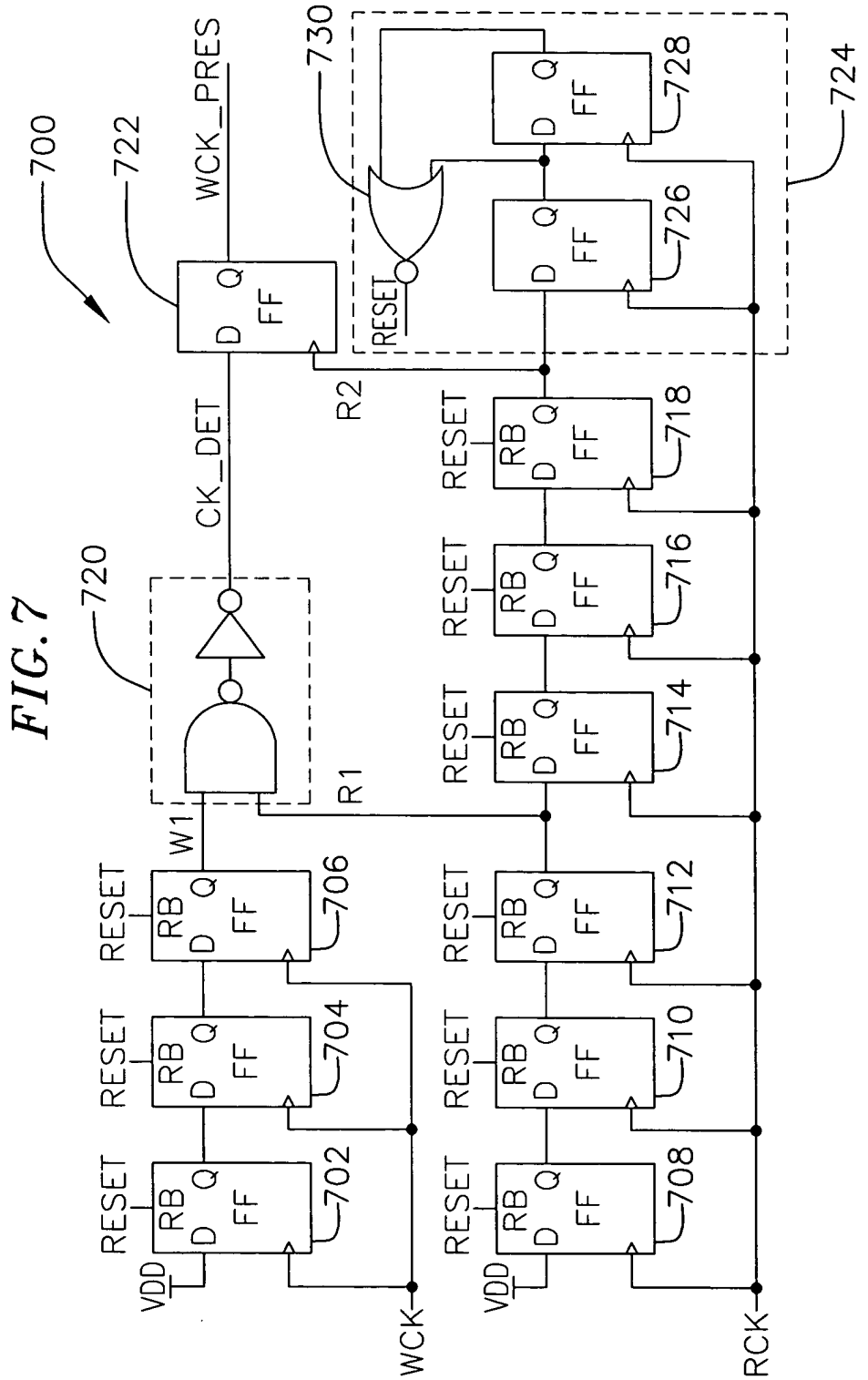

600
504
HOLD
CKPRES
LCKDET
CLOCK PRESENT DETECTOR
502
604
SEL
A MUX B
RCKDIV2
D QB FF
602
RCK
RCK
WCK
512
RRSTB
514
RB D Q FF
510
RCK
508
RB D Q FF
RCK
SEL
A MUX B
610
612
HOLD
RB D Q FF
RCK
HOLD
RB D Q FF
506
RSTB
WCK
522
WRSTB
520
518
HOLD
RB D Q FF
516
HOLD
RB D Q FF
M U X
SEL
606
WCK

FIG. 6

FIG. 7


700
722
WCK_PRES
730
724
728
726
RESET
R2
CK_DET
720
718
716
714
R1
W1
706
712
704
710
702
708
VDD
WCK
RCK

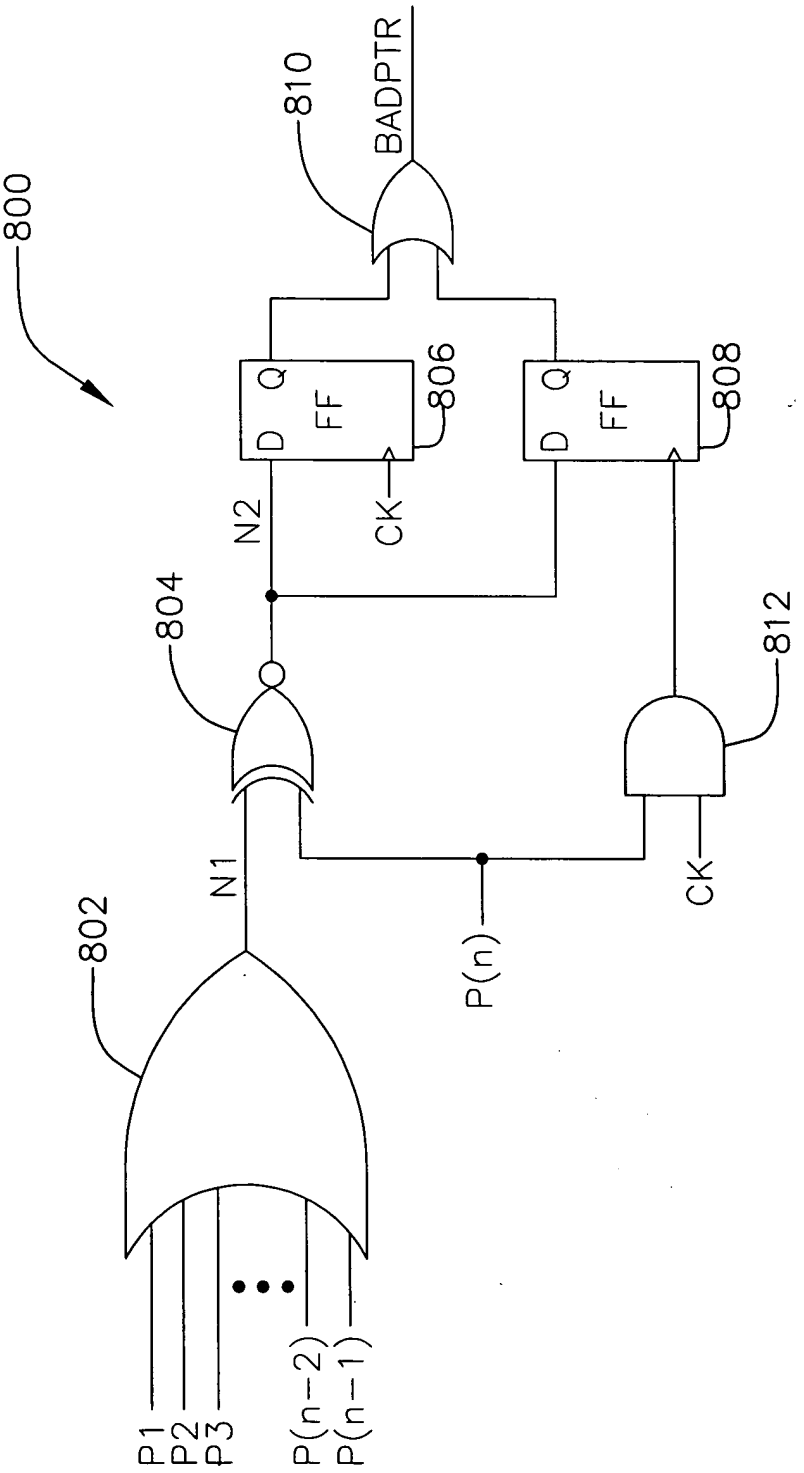

800
810
BADPTR
806
808
D Q
FF
CK
N2
804
812
N1
802
P(n)
P1
P2
P3
P(n-2)
P(n-1)

FIG. 8